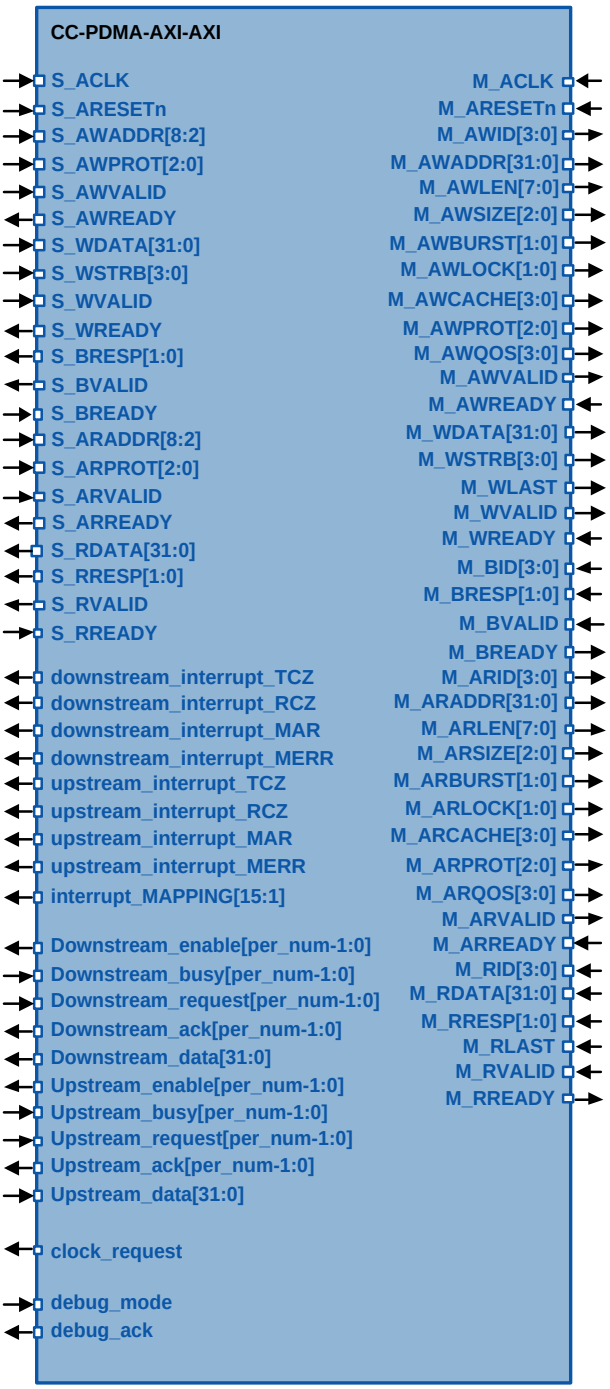
CC-PDMA-AXI-AXI Peripheral Direct Memory Access Controller

Symbol



Features

- AMBA AXI4-Lite slave bus
- AMBA AXI4 master bus
- Configurable number of peripheral channels
- 8, 16, 32 bits data transfer modes
- Upstream and downstream data aggregation to 32 bit chunks
- Various address modes
- Various arbiter priority schemes
- Circular buffer support
- Configurable independent upstream and downstream FIFOs
- Maskable interrupts
- Dedicated upstream and downstream peripherals DMA interface
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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Generic Parameters

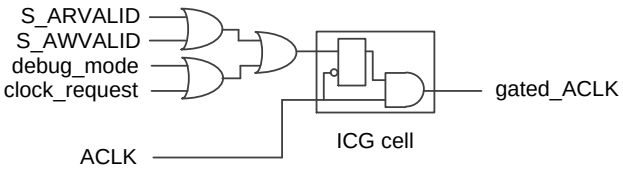
Generic name	Description	Type	Range
reg_ADDR_width	APB PADDR signal width	integer	1:32
peripherals_numer	Configure number of peripherals	integer	1:32
peripheral_select _width	Width of the peripheral select register	integer	1:5
downstream_channel _number	Number of downstream channels	integer	1:32
downstream_channel _number_width	Downstream channels number width	integer	1:5
upstream_channel _number	Number of upstream channels	integer	1:32
upstream_channel _number_width	Upstream channels number width	integer	1:5
downstream_data _aggregation _and_FIFO_enable	Enable downstream data aggregation	integer	0, 1
downstream_fifo _depth	Downstream FIFO depth	integer	0:32
downstream_fifo _depth_width	Downstream FIFO depth width	integer	0:5
upstream_data _aggregarion_enable	Enable upstream data aggregation	integer	0, 1
upstream_fifo _depth	Upstream FIFO depth	integer	0:32
upstream_fifo _depth_width	Upstream FIFO depth width	integer	0:5
upstream_fifo_water _level	Water level of upstream FIFO	integer	0:32
default_interrupt _MAPPING	Reset value of interrupt_MAPPING register	integer	0:32767
LOAD_DELAY	Additional register DMA channel output data	integer	0, 1
AWID	Passed to the AXI master AWID	integer	0:15
AWCACHE	Passed to the AXI master AWCACHE	integer	0:15
AWQOS	Passed to the AXI master AWQOS	integer	0:15
BID	Passed to the AXI master BID	integer	0:15
ARID	Passed to the AXI master ARID	integer	0:15
ARCACHE	Passed to the AXI master ARCACHE	integer	0:15
ARQOS	Passed to the AXI master ARQOS	integer	0:15
RID	Passed to the AXI master RID	integer	0:15

Pin-out Description

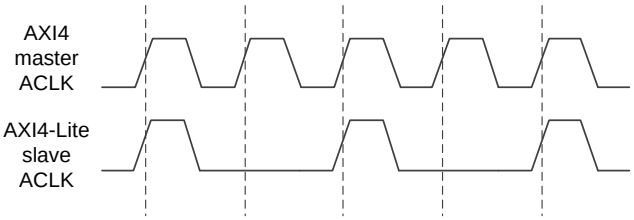
Pin name	Description	I/O	Active
AMBA AXI4-Lite slave signals			
S_ACLK	Synchronous clock	I	rising
S_ARESETn	Asynchronous reset	I	low
S_AWADDR [reg_ADDR_width+1:2]	AXI write address	I	data
S_AWPROT[2:0]	AXI write address protection type	I	Data
S_AWVALID	AXI write address valid	I	high
S_AWREADY	AXI write address ready	O	high
S_WDATA[31:0]	AXI write data	I	data
S_WSTRB[3:0]	AXI write strobe	I	high
S_WVALID	AXI write valid	I	high
S_WREADY	AXI write ready	O	high
S_BRESP[1:0]	AXI write response	O	data
S_BVALID	AXI write response valid	O	high
S_BREADY	AXI write response ready	I	high
S_ARADDR [reg_ADDR_width+1:2]	AXI read address	I	data
S_ARPROT[2:0]	AXI read address protection type	I	data
S_ARVALID	AXI read address valid	I	High
S_ARREADY	AXI read address ready	O	high
S_RDATA[31:0]	AXI read data	O	data
S_RRESP[1:0]	AXI read response	O	data
S_RVALID	AXI read valid	O	high
S_RREADY	AXI read ready	I	high
Interrupt signals			
downstream _interrupt_TCZ	Transfer counter zero interrupt	O	high
downstream interrupt_RCZ	Reload counter zero interrupt	O	high
downstream interrupt_MAR	Memory address reloaded interrupt	O	high
downstream interrupt_MERR	Memory access error interrupt	O	high
upstream _interrupt_TCZ	Transfer counter zero interrupt	O	high
upstream interrupt_RCZ	Reload counter zero interrupt	O	high
upstream interrupt_MAR	Memory address reloaded interrupt	O	high
upstream interrupt_MERR	Memory access error interrupt	O	high
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data
Downstream_enable [peripherals_numer-1:0]	PDMA downstream enable signal	O	high

Integration example

- Using clock_request pin for low power mode:



- Using different clock ratio for AMBA AXI4 master and slave buses:



PDMA signals			
Downstream_busy [peripherals_numer-1:0]	PDMA downstream busy signal	I	high
Downstram_request [peripherals_numer-1:0]	PDMA downstream request signal	I	high
Downstream_ack [peripherals_numer-1:0]	PDMA downstream acknowledge signal	O	high
Downstream_data[31:0]	PDMA downstream data	O	data
Upstream_enable [peripherals_numer-1:0]	PDMA upstream enable signal	O	high
Upstream_busy [peripherals_numer-1:0]	PDMA upstream busy signal	I	high
Upstram_request [peripherals_numer-1:0]	PDMA uptream request signal	I	high
Upstream_ack [peripherals_numer-1:0]	PDMA upstream acknowledge signal	O	high
Upstream_data[31:0]	PDMA upstream data	I	data
Debug and power management signals			
clock_request	Clock request signal	O	high
debug_mode	Debug mode input	I	high
debug_ack	Debug mode acknowledge	O	high

AMBA AXI4 master signals			
M_ACLK	Synchronous clock	I	rising
M_ARESETn	Asynchronous reset	I	low
M_AWID[3:0]	AXI write address ID	O	data
M_AWADDR[31:]	AXI write address	O	data
M_AWLEN[7:0]	AXI write burst length	O	data
M_AWSIZE[2:0]	AXI write burst size	O	data
M_AWBURST[1:0]	AXI write burst type	O	data
M_AWLOCK[1:0]	AXI write lock type	O	data
M_AWCACHE[3:0]	AXI write memory type	O	data
M_AWPROT[2:0]	AXI write address protection type	O	data
M_AWQOS[3:0]	AXI write Quality of Service	O	data
M_AWVALID	AXI write address valid	O	high
M_AWREADY	AXI write address ready	I	high
M_WDATA[31:0]	AXI write data	O	data
M_WSTRB[3:0]	AXI write strobe	O	high
M_WLAST	AXI write last	O	high
M_WVALID	AXI write valid	O	high
M_WREADY	AXI write ready	I	high
M_BID[3:0]	AXI write response ID	I	data
M_BRESP[1:0]	AXI write response	I	data
M_BVALID	AXI write response valid	I	high
M_BREADY	AXI write response ready	O	high
M_ARID	AXI read address ID	O	data
M_ARADDR[31:0]	AXI read address	O	data
M_ARLEN[7:0]	AXI read burst length	O	data
M_ARSIZE[2:0]	AXI read burst size	O	data
M_ARBURST[1:0]	AXI read burst type	O	data
M_ARLOCK[1:0]	AXI read lock type	O	data
M_ARCACHE[3:0]	AXI read memory type	O	data
M_ARPROT[2:0]	AXI read protection type	O	data
M_ARQOS[3:0]	AXI read Quality of Service	O	data
M_ARVALID	AXI read address valid	O	high
M_ARREADY	AXI read address ready	I	high
M_RID	AXI read response ID	I	data
M_RDATA[31:0]	AXI read data	I	data
M_RRESP[1:0]	AXI read response	I	data
M_RLAST	AXI read last	I	high
M_RVALID	AXI read valid	I	high
M_RREADY	AXI read ready	O	high

Block Diagram