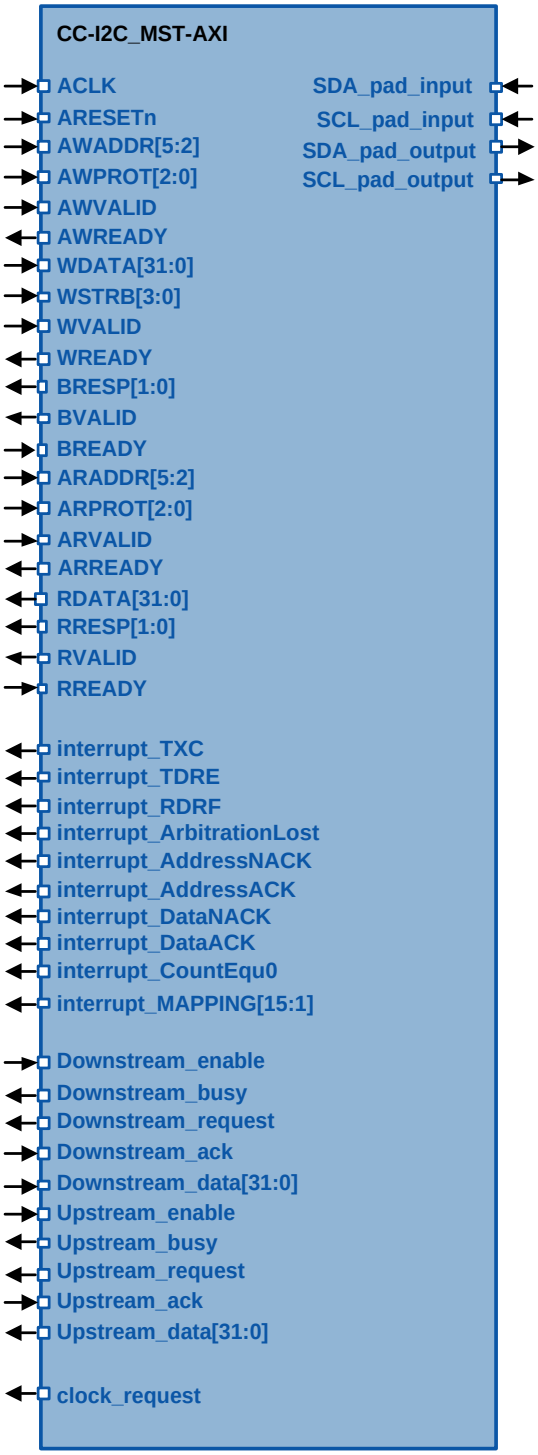
CC-I2C_MST-AXI I2C Master Serial Interface Controller

Symbol



Features

- I2C-compatible interface
- AMBA AXI4-Lite bus
- Standard and custom data rates
- Configurable setup/hold times
- Multi-master support
- Clock stretching support
- Programmable SDA/SCL input filter
- Automatic Start, Stop, Repeated Start, Acknowledge support
- 7 and 10 bit addressing format support
- Maskable interrupts
- Dedicated upstream and downstream DMA interface
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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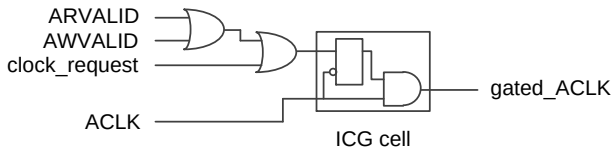
Generic Parameters

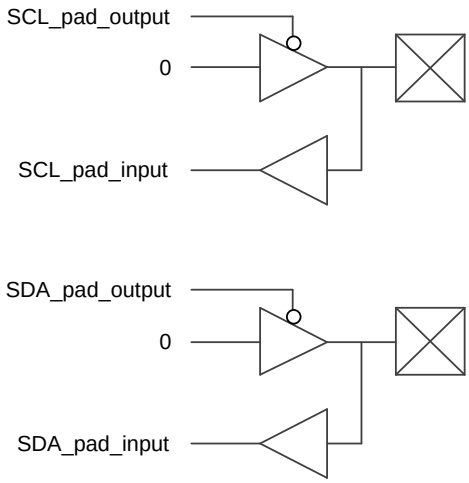
Generic name	Description	Type	Range
PDMA_support	Configure PDMA interface support	integer	0, 1
i2cPrescalerWidth	Configure clock prescaler width	integer	1:32
i2cCountWidth	Configure data counter width	integer	1:32
default_interrupt _MAPPING	Reset value of interrupt_MAPPING register	integer	0:32767

Integration example

- Using clock_request pin for low power mode:



- Pad connection example:



Pin-out Description

Pin name	Description	I/O	Active
ACLK	Synchronous clock	I	rising
ARESETn	Asynchronous reset	I	low
AWADDR[5:2]	AXI write address	I	data
AWPROT[2:0]	AXI write address protection type	I	data
AWVALID	AXI write address valid	I	high
AWREADY	AXI write address ready	O	high
WDATA[31:0]	AXI write data	I	data
WSTRB[3:0]	AXI write strobe	I	high
WVALID	AXI write valid	I	high
WREADY	AXI write ready	O	high
BRESP[1:0]	AXI write response	O	data
BVALID	AXI write response valid	O	high
BREADY	AXI write response ready	I	high
ARADDR[5:2]	AXI read address	I	data
ARPROT[2:0]	AXI read address protection type	I	data
ARVALID	AXI read address valid	I	High
ARREADY	AXI read address ready	O	high
RDATA[31:0]	AXI read data	O	data
RRESP[1:0]	AXI read response	O	data
RVALID	AXI read valid	O	high
RREADY	AXI read ready	I	high
interrupt_TXC	Transmission complete interrupt	O	high
interrupt_TDRE	Transmit data register empty interrupt	O	high
interrupt_RDRF	Read data register full interrupt	O	high
interrupt_ArbitrationLost	Arbitration lost interrupt	O	high
interrupt_AddressNACK	Address NACK interrupt	O	high
interrupt_AddressACK	Address ACK interrupt	O	high
interrupt_DataNACK	Data NACK interrupt	O	high
interrupt_dataACK	Data ACK interrupt	O	high
Interrupt_CountEqu0	Count equals zero interrupt	O	high
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data
Downstream_enable	PDMA downstream enable signal	I	high
Downstream_busy	PDMA downstream busy signal	O	high
Downstram_request	PDMA downstream request signal	O	high
Downstream_ack	PDMA downstream ack signal	I	high
Downstream_data[31:0]	PDMA downstream data	I	data
Upstream_enable	PDMA upstream enable signal	I	high
Upstream_busy	PDMA upstream busy signal	O	high
Upstram_request	PDMA uptream request signal	O	high
Upstream_ack	PDMA upstream ack signal	I	high

Upstream_data[31:0]	PDMA upstream data	O	data
clock_request	Clock request signal	O	high
SDA_pad_input	I2C data pin input	I	As I2C spec.
SCL_pad_input	I2C clock pin input	I	As I2C spec.
SDA_pad_output	I2C data pin output	O	As I2C spec.
SCL_pad_output	I2C clock pin output	O	As I2C spec.