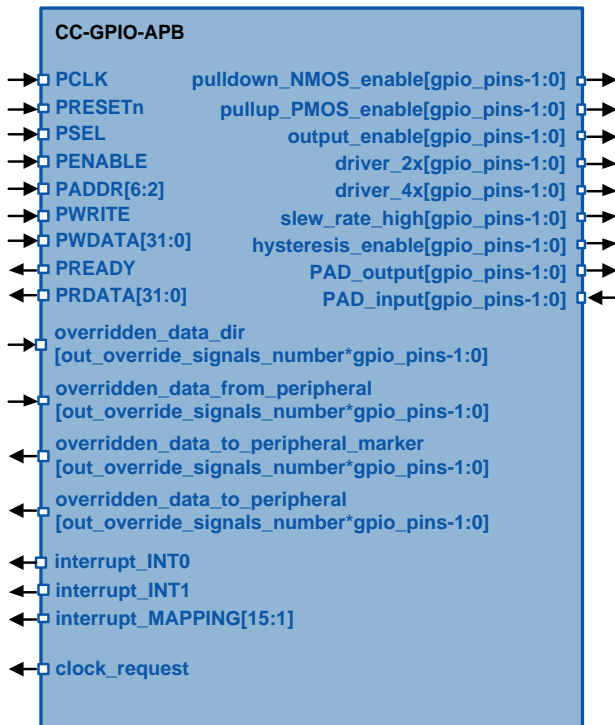


## CC-GPIO-APB General Purpose Input/Output Controller

### Symbol



### Features

- AMBA APB3 bus
- Individual configuration of each GPIO pin
- Dynamic programming of each GPIO pin as input or output
- Configurable level or edge triggered interrupts
- Alternative functions support
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

### Benefits

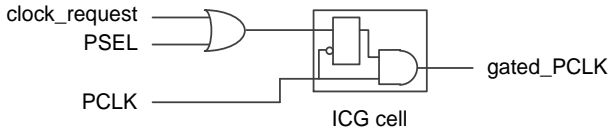
- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

## Generic Parameters

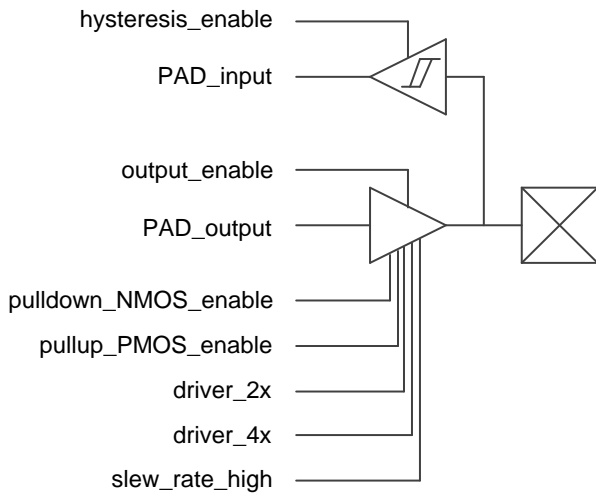
| Generic name                | Description                                    | Type    | Range   |
|-----------------------------|--|---------|---------|
| gpio_pins                   | Number of GPIO pins                            | integer | 1:32    |
| out_override_signals_number | Number of GPIO alternative functions           | integer | 0, 1, 3 |
| out_override_select_width   | Width of alternative functions select register | integer | 0, 1, 2 |
| default_interrupt_MAPPING   | Reset value of interrupt_MAPPING register      | integer | 0:32767 |

## Integration example

- Using clock\_request pin for low power mode:



- Pad connection example:



## Pin-out Description

| Pin name  | Description                                 | I/O | Active |
|---|---|-----|--------|
| PCLK  | Synchronous clock                           | I   | rising |
| PRESETn   | Asynchronous reset                          | I   | low    |
| PSEL  | APB peripheral select                       | I   | high   |
| PENABLE   | APB bus enable                              | I   | high   |
| PADDR[6:2]  | APB bus address                             | I   | data   |
| PWRITE  | APB bus write                               | I   | high   |
| PWDATA[31:0]  | APB bus write data                          | I   | data   |
| PREADY  | APB bus ready                               | O   | high   |
| PRDATA[31:0]  | APB bus read data                           | O   | data   |
| pullup_NMOS_enable [gpio_pins-1:0]  | Pull down enable signal                     | O   | high   |
| pullup_PMOS_enable [gpio_pins-1:0]  | Pull up enable signal                       | O   | high   |
| output_enable [gpio_pins-1:0]   | Output enable signal                        | O   | high   |
| driver_2x [gpio_pins-1:0]   | Driver 2x selection signal                  | O   | high   |
| driver_4x [gpio_pins-1:0]   | Driver 4x selection signal                  | O   | high   |
| slew_rate_high [gpio_pins-1:0]  | High slew rate enable signal                | O   | high   |
| hysteresis_enable [gpio_pins-1:0]   | Hysteresis enable signal                    | O   | high   |
| PAD_output [gpio_pins-1:0]  | Driver output signal                        | O   | data   |
| PAD_input [gpio_pins-1:0]   | Pad input signal                            | I   | data   |
| overridden_data_dir [out_override_signals_number *gpio_pins-1 : 0]                  | Alternative functions direction signal      | I   | high   |
| overridden_data_from_peripheral [out_override_signals_number *gpio_pins-1 : 0]      | Alternative functions data from peripherals | I   | data   |
| overridden_data_to_peripheral_marker [out_override_signals_number *gpio_pins-1 : 0] | Alternative functions selection marker      | O   | high   |
| overridden_data_to_peripheral [gpio_pins-1:0]                                       | Alternative functions data to peripherals   | O   | data   |
| interrupt_INT0  | INT0 interrupt line                         | O   | high   |
| interrupt_INT1  | INT1 interrupt line                         | O   | high   |
| interrupt_MAPPING[15:1]   | Interrupt mapping vector                    | O   | data   |
| clock_request   | Clock request signal                        | O   | high   |



# Internal GPIO pin structure

